Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RUDIGER KLETTE

Appeal No. 2002-1854
Application No. 09/163,874

ON BRIEF

Before ABRAMS, FRANKFORT, and BAHR, Administrative Patent Judges.

ABRAMS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1-4, which are all of the claims pending in this application.[1]

We REVERSE.

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[1]Claim 1 was amended after the final rejection.

BACKGROUND

The appellant's invention relates to a method for the linear configuration of metallic fuse sections. An understanding of the invention can be derived from a reading of exemplary claim 1, which has been reproduced below.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Nakaizumi	4,985,866	Jan. 15, 1991

Claims 1-4 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nakaizumi.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellant regarding the above-noted rejection, we make reference to the Answer (Paper No. 17) for the examiner's complete reasoning in support of the rejection, and to the Brief (Paper No. 16) and Reply Brief (Paper No. 18) for the appellant's arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellant's specification and claims, to the applied prior art reference, and to the respective positions articulated by the appellant and the examiner. As a consequence of our review, we make the determinations which follow.

The appellant's invention is directed to a method for the linear configuration of metallic fuse sections which provide a bit combination that represents a characteristic of a circuit on a wafer. As explained in the opening pages of the specification, selected fuse sections in a linear arrangement are burned (severed) to set the characteristics of circuits. These fuse sections can only be accessed for such action when the polyimide passivation layer that covers them after they are assembled into an arrangement has been removed by exposure and etching. According to the appellant, while under optimum process conditions the polyimide layer is completely removed from all of the fuse sections in an arrangement, under unfavorable conditions it may be that the layer remains over the fuse section that represents the most significant bit (number) of a bit combination that will set the circuit. This prevents that fuse section from being burned without further actions being taken to uncover it, which complicates the manufacturing process. The appellant states that it is common for the polyimide layer not to be removed from the end portions of a line of fuse sections in an arrangement, and therefore if a fuse section that must be burned in order to construct the circuit is located in an end portion, it cannot be accessed in order to be burned. See pages 12, 8 and 9; Figures 2 and 3. The objective of the appellant's invention is to minimize this problem, which is accomplished by placing a fuse section that has been selected as being significant to the establishment of the desired circuit and placing it at a location other than in the end portion of the configuration of fuse sections.

Claim 1 sets forth the invention in the following manner:

1. In a method for the linear configuration of metallic fuse sections, the improvement which comprises:

providing a fuse with fuse sections in a linear configuration, said fuse sections having a bit combination;

selecting a fuse section corresponding to the most significant bit; and

placing other fuse sections adjacent both sides of the fuse section corresponding to the most significant bit.

The examiner has rejected claim 1 as being anticipated by Nakaizumi. In arriving at this conclusion, the examiner has focused upon lines 46-57 and Figure 3 of the reference, contending that all of the steps in claim 1 are taught therein. The appellant argues in rebuttal that while Nakaizumi might arrange a plurality of fuse sections in a linear configuration, it does not disclose or teach the steps of selecting a fuse section corresponding to the moist significant bit and placing the other fuse sections adjacent both sides of the selected fuse section.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of the claimed invention. See, for example, RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the

invention. In re Graves, 69 F.3d 1147, 1152, 36 USPQ2d 1697, 1701 (Fed. Cir. 1995), cert. denied, 116 S.Ct. 1362 (1996), quoting from In re LeGrice, 301 F.2d 929, 936, 133 USPQ 365, 372 (CCPA 1962). Applying this guidance of our reviewing court leads us to conclude that the rejection cannot be sustained. Our reasoning follows.

Nakaizumi is directed to a semiconductor memory device having redundant circuit configuration. As explained in the opening paragraphs, systems existed in the prior art in which defective memory cells could be replaced by good cells held available in a bank of redundant cells. The required redundant cells were brought on line by burning selected fuses. The objective of this reference is to improve upon such prior art systems.

The examiner does not focus upon the improvement provided by the reference. In the portion of Nakaizumi to which the examiner refers, the patentee explains that a plurality of primary word address decoders are arrayed, that six signals are selected for input to the decoders under different combinations, and that only one is selected and inputted to a word line W. A concise explanation of the operation of the system is found in column 7, where with reference to Figures 4 and 6, it is explained that in normal operation the fuse element 121 (Figure 4) is intact, and the decoder in word line W_J is in use, but if that decoder becomes defective the system reacts by causing fuse element 121 to be blown by a laser beam, which causes a decoder from redundant line W_R to be brought into use.

We do not agree with the examiner that the Nakaizumi system anticipates the subject matter recited in claim 1. It is true that certain decoders are selected for use and that, as shown in Figures 3, 4 and 7, the system includes a plurality of fuses 91-102 arranged in a linear array. However, we find ourselves in agreement with the appellant that the reference neither selects a fuse section corresponding to the most significant bit nor places other fuse sections adjacent both sides of the selected fuse section. Furthermore, the reference fails to recognize the specific problem to which the appellant's invention is directed. In fact, Nakaizumi is not at all concerned with the arrangement of the fuse sections with respect to one another, but only that redundant sections are present and can be substituted for sections associated with failed decoders.

Since all of the subject matter recited in claim 1 is not disclosed or taught by Nakaizumi, the reference does not anticipate the claim, and we will not sustain the rejection. Nor, it follows, will we sustain the like rejection of claims 2-4, which depend from claim 1.

CONCLUSION

The rejection is not sustained.

The decision of the examiner is reversed.

REVERSED

NEAL E. ABRAMS Administrative Patent Judge	)))))) BOARD OF PATENT
CHARLES E. FRANKFORT Administrative Patent Judge	) APPEALS AND) INTERFERENCES
JENNIFER D. BAHR Administrative Patent Judge	))))))

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